ELECTRICAL ENGINEERING

An area efficient high speed, fully on-chip low dropout -LDO- voltage regulator

INGENIERIA ELECTRICA

Regulador de Voltaje -LDO- completamente integrado de baja caída de tensión, alta velocidad y bajo consumo de área.

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Resumen

Este artículo presenta el diseño de un regulador de voltaje de baja caída de tensión, el cual presenta un bajo consumo de potencia y área, así como una respuesta transitoria optimizada. La reducción en área se logra mediante la polarización del transistor de potencia en la región de triodo. Así mismo, se hace uso de una red de polarización dinámica con el propósito de reducir a 300ns el tiempo de establecimiento para cualquier cambio en la corriente de carga (desde 100μA hasta 100mA). El regulador es diseñado en la tecnología Silterra CMOS estándar de 0.18μm, y proporciona un voltaje regulado de 1.8V. Todo el circuito es polarizado únicamente con 2.3μA para cargas inferiores a 1mA, y puede recuperarse en 0.3μs para cualquier cambio en la carga y voltaje de entrada. Además, el regulador no necesita de ningún capacitor externo para garantizar su estabilidad.

Palabras clave: Polarización adaptativa, polarización dinámica, regulador lineal, respuesta transitoria, sin capacitor de salida.

Abstract

This paper presents the design of a low-dropout voltage regulator which has a low area and power consumption, as well as an improved transient response. The area reduction is achieved by biasing the power transistor in the triode region. In addition, a dynamic bias network is used in order to reduce its settling time to 300ns for any change in the load current from 100μA to 100mA. The regulator is designed in a Silterra 0.18μm standard CMOS technology and brings a regulated output voltage of 1.8V. All the circuit is biased with 2.3μA only at loads smaller than 1mA, and can recover within 0.3μs for maximum load and input voltage changes. Moreover, the regulator does not need any external capacitor to guarantee its stability.

Keywords: Adaptive bias, dynamic bias, linear regulator, output capacitor less, transient response.

1. Introduction

Power management system has an important role on the performance of any mixed-signal circuit (Rincon, 2009). One of its tasks is to extend the battery life and therefore the operating time of the device, varying between different supply voltages depending on the activity of the chip. System on chip (SoC) is a common solution to integrate many functions that can switch simultaneously with the clock. Switching of numerous devices demands both high power and fast response times. Therefore, integrated circuits need regulators in power management in order to avoid substantial voltage and current variations across time and over a wide range of operating conditions (Lam & Ki, 2008; Rincon, 2009).

Regulators can be classified in linear and switching. Switching regulators has a mixed signal nature combining analog and digital functions (Chia, et al., 2012). On another hand, linear regulators linearly modulate a conductance of a series pass switch connected between the input and the output of the circuit, being faster and less noisy than switching counterpart (Rincon, 2009). Low-dropout regulators (LDO) are a type of linear regulators very common in many power management systems, because they can produce a ripple-free output voltage with short transient responses, even considering fast load changes such as high speed memories.

A LDO regulator can be seen as a negative-feedback amplifier composed by two or more single stages, in which each one is biased in the saturation region typically, in order to develop a high speed and gain. However, to achieve a low-dropout voltage, the aspect ratio of the power transistor —the last stage— could be greater than 40000 for a load current of 100mA (Lovaraju, et al., 2013; Ming, et al., 2012), which implies a large area consumption as well as a large parasitic capacitance (Gutierrez, 2008). In addition, parameters such as transconductance and output impedance of the power transistor vary more than 500% between full-load and light-load conditions, producing that the open-loop gain, phase margin and GBW of the regulator change dramatically; this could affect the stability of the circuit for any load changes (Man, et

al., 2008). To overcome these problems, a common alternative is to use a capacitance at the output of the LDO to ensure stability and reduce voltage spikes. However, due to its high value (several picofarads or almost nanofarad), this capacitance needs to be an external component, reducing the bandwidth of the regulator.

For those reasons, in this paper the design of low area and high speed LDO regulator is presented. The area improvement is achieved due to the use of a power transistor biased in the triode region. Also, dynamic and adaptive bias schemes, as well as a high slew-rate differential pair, are used in order to reduce the settling time of the circuit for any load and input voltage variation. In addition, the stability of the regulator is ensured by using indirect compensation avoiding the need of external components.

2. Voltage regulator topology

Figure 1 shows the topology of the designed regulator. It consists of an error amplifier, a power transistor, and dynamic and adaptive biasing networks.
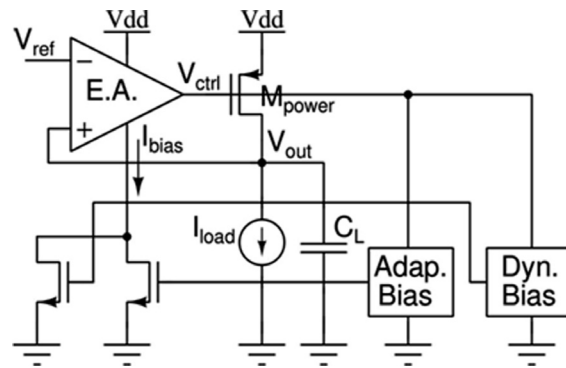

Figure 1. *Proposed LDO regulator.*

2.1 Power transistor

The basic equation for the drain current of a MOSFET in saturation is:

$$I_{DS} = \frac{1}{2} K_P \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{1}{2} K_P \frac{W}{L} V_{OV}^2 \qquad (1)$$

The dropout voltage of the regulator is the drain-to-source voltage V_{DS} of the power transistor M_{Power}, and its minimum value corresponds to the overdrive

voltage V_{OV} of equation 1. Therefore, in order to provide a high output current with a low dropout voltage —which means a low overdrive— a very high aspect ratio W/L is needed. This implies large area consumption as well as parasitic capacitances.

On the other hand, the relationship between the drain current and V_{GS} and V_{DS} in the triode region is:

$$I_{DS} = K_P \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right) \qquad (2)$$

So, for a given V_{DS}—dropout voltage— there is not necessary to increase the aspect ratio W/L because there is another degree of freedom corresponding to V_{GS}. Hence, it is possible to minimize the area of the power transistor by applying a high V_{GS}.

2.2 Error amplifier

The error amplifier is a one-stage current mirror OTA, as figure 2 shows. We propose the use of a source-cross-coupled differential pair as the input stage composed by $M_{1,2,3,4}$ and $M_{13,14,15,16}$ (Baker, 2010). Its main advantage is the high slew-rate that it can achieve using a very low quiescent current needed to drive the input capacitance of the power transistor. In many common amplifiers the slew-rate is limited by the bias current of both the input differential pair and output branch; then, for driving high capacitive loads it is necessary to use an output-stage as a class AB one (Rijns & Wallinga, 1990; Yavari, 2010). However, in a source-cross-coupled amplifier the tail current depends on the amplitude of the input signal: if V_{in+} is much higher than V_{in-} —the slewing condition— the current through M_2 and M_3 does not copy the current from M_{15} and rises without any limit; then, the current of M_{21} and M_{20} increases too, providing a high slew-rate at the output node. When the transient state finishes, the gate voltage of $M_{1,13}$ and $M_{2,14}$ tends to be equal, and the current flowing through the pair is set by the current mirror composed by $M_{17,18,19}$ i.e. by the source I_{REF}. This reference can be set as low as the needed to guaranty a maximum steady-state error and noise level, thus minimizing the power consumption.

Finally, capacitors C_{C1} and C_{C2} are used to compensate the regulator. The circuit uses indirect miller compensation due to the high variation in both gain and bandwidth with load. Transistors $M_{20,21}$ and $M_{22,23}$ —compound transistors— forms the low-impedance node and current buffer which are needed to eliminate the right-plane zero; therefore, phase and gain margin are improved.
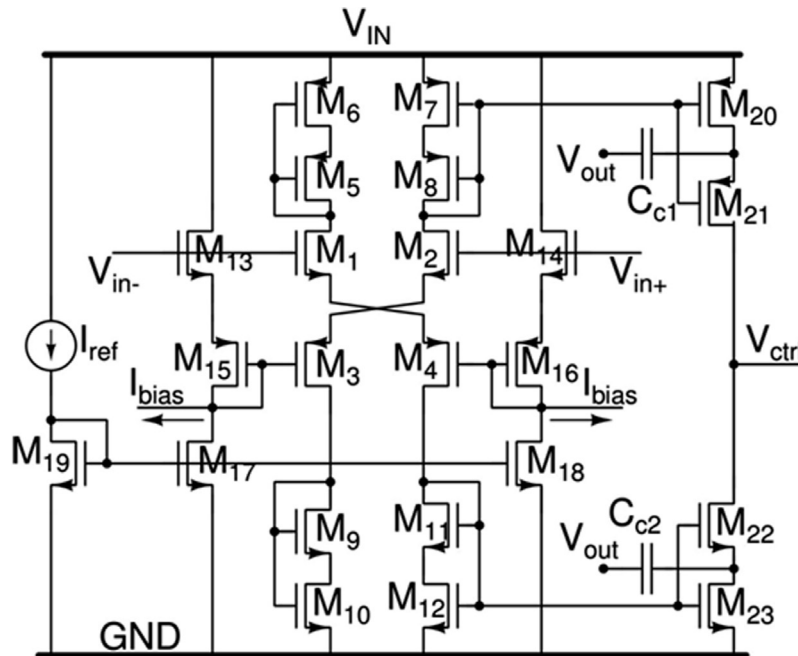

Figure 2. Circuit diagram of the Error Amplifier.

3. Dynamic and adaptive biasing

The fact of using a power transistor biased in triode region to deliver the output current of the regulator implies that the circuit could have a lower bandwidth and therefore a higher settling time. A triode-MOSFET-transistor develops almost five times less transconductance than a saturated device; so, recovery time as well as open-loop gain can be compromised.

Figure 3 shows a dynamic bias scheme —$M_{(26...29)}$ (Ho, et al., 2011) and $M_{31,33}$—, as well as an adaptive one —$M_{24,25}$ and $M_{30,32}$—. When the regulator is fully loaded (100mA) the power transistor is in triode region, so the bandwidth of the circuit is reduced. But, in the presence of a fast load change i. e. from 100mA to 100µA in 100ns, transistors M_{31} and M_{33} add some extra current to the bias branches of the error amplifier in order to increase even more its slew-rate and discharge the gate capacitance of M_P quickly. This extra current is controlled by the voltage of the resistor R_{HP}, which is the output of a passive first-order high-pass filter. We propose to use two logic inverters —formed by $M_{(26...29)}$— in order to regenerate the control signal of M_P in a shorter time than the given by the bandwidth of the regulator i.e. in a few nanoseconds; then the high-pass filter transmits this signal to the gate of M_{31} to increase the bias current. Once the output voltage has settled down, the output of the passive

filter will be zero, and no extra current is added to the error amplifier. It is important to highlight that there will flow current only through M_{31} during the discharge transient response of the circuit, thus the current consumption in steady state is minimized.

When the output current increases from 100µA to 100mA the adaptive bias network add more bias current to the error amplifier, with the same purpose of increase even more its slew-rate. This adaptive network forms another negative-feedback that helps to increase the bandwidth of the loop and to reduce the settling time of the regulator. It is important to emphasize that the copy ratio between M_P and M_{25} has to be very low i.e. 10000/1, in order to reduce the quiescent power consumption and enhance the gain of the error amplifier.

4. Simulation results

Simulations were performed using a Silterra 180nm standard CMOS technology, with a power supply of 2 V and a reference and output regulated voltage of 1.8 V. The overall current consumption was only 2.3 µA for no load condition. The power transistors dimensions were 1.5 mm/180 nm which is much lower than many LDO reported (Lovaraju et al., 2013; Ming et al., 2012). In order to validate the specifications, transient simulations are the best option to show more approximate performance. Line and load transient simulation should be made
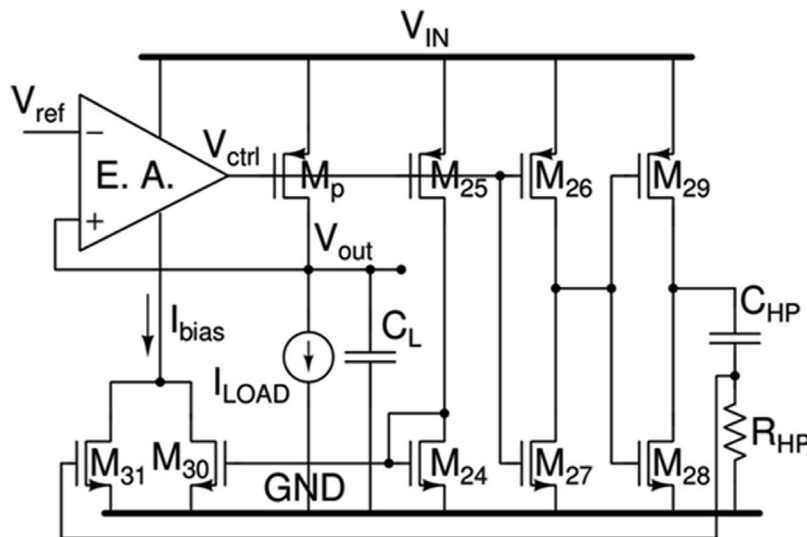

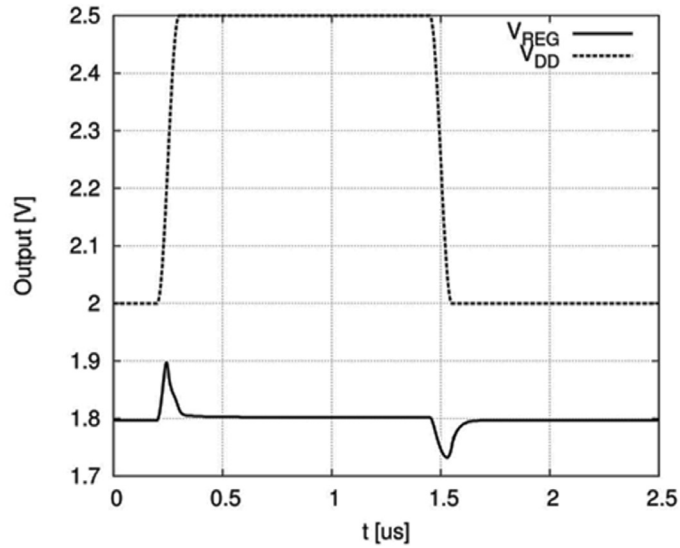***Figure 3.*** *Circuit diagram of the proposed LDO regulator.*

Figure 4. *Line transient response.*

varying power supply and load current respectively. The rise and fall times of the variables are set in values according other papers and for high speed response. Finally, DC simulation is made to validate the operating point according transient results.

Line and load transient response were obtained to validate the performance of the proposed regulator where rise and fall times used were 100 ns is all simulations. Figure 4 shows the line response for a power supply change from 2 to 2.5 V. It can be seen the output regulated voltage reaches steady state very fast with a maximum time in

the positive edge of the input (V_DD) of 300 ns probing the stability of the circuit respect power supply variations. The under and overshoot of output voltage do not exceed 100 mV in any case.

Figure 6 shows the load response for a current load variation from 100 μA to 100 mA. It probes the correct operation of dynamic and adaptive bias; despite having low quiescent current, because of the high slew-rate, the output voltage reach the steady state in less than 300 ns considering 1% settling time for positive and negative edge of the load current. Also, circuit stability is ensured
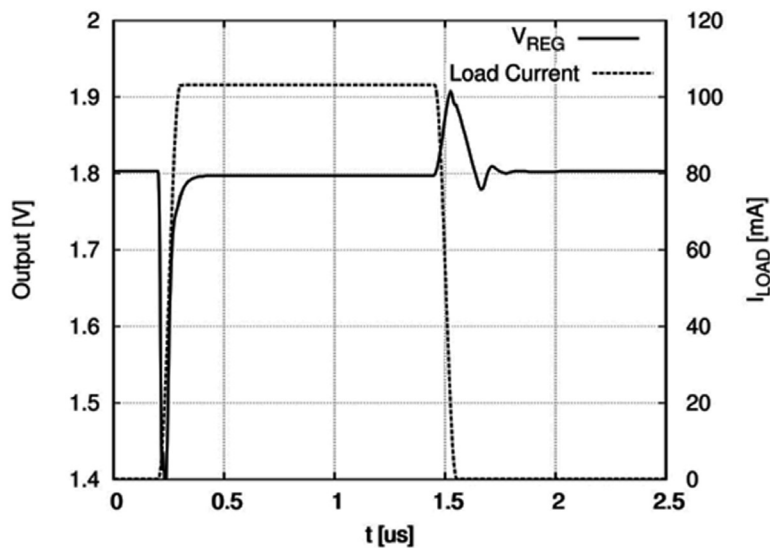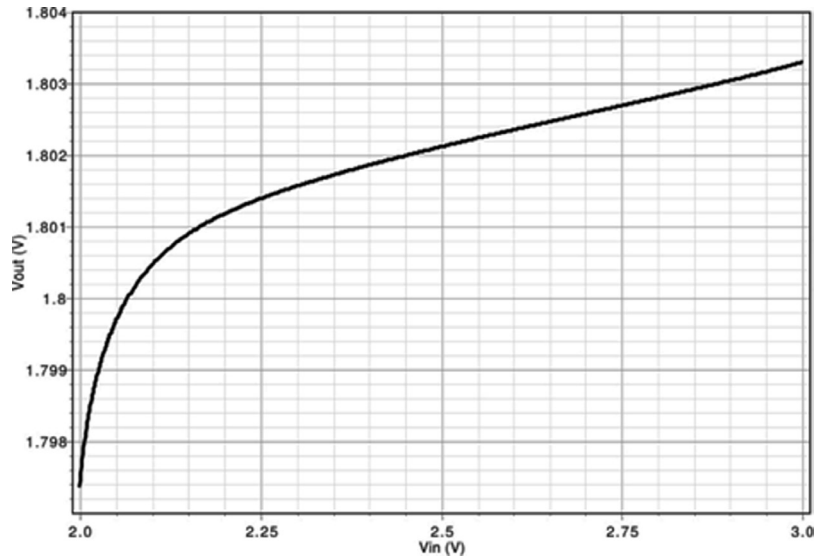

Figure 5. *Load transient response.*

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Figure 6. *Line regulation.*

for different load capacitance from 0 to 100 pF avoiding the use of external large capacitors. Overshoot voltage does not reach 150 mV while undershoot is more critical reaching 400 mV.

Figure 6 shows line DC response of the regulator varying power supply from 2 to 3 V where the change in the output regulated voltage is around 5 mV; it means a line regulation of 5 mV/V. On another hand, load DC response is shown in Figure 7, where the variations of the load from 100 μA to 100 mA results in a load regulation of 0.06 mV/mA.

Finally, Table 1 summarizes the specifications of the proposed LDO. Some circuits found in the literature are included. The main idea of this work was to keep in a low value the settling time while reducing power consumption. Table 1 shows that the settling time is in the order of other works accomplishing the first target. In addition, the current consumption is the lowest. This result is obtained by reducing the complex circuitry used in others works in order to improve the performance. By keeping the simplicity of the circuit, less elements can be used and thus reducing the current consumption. Finally, the
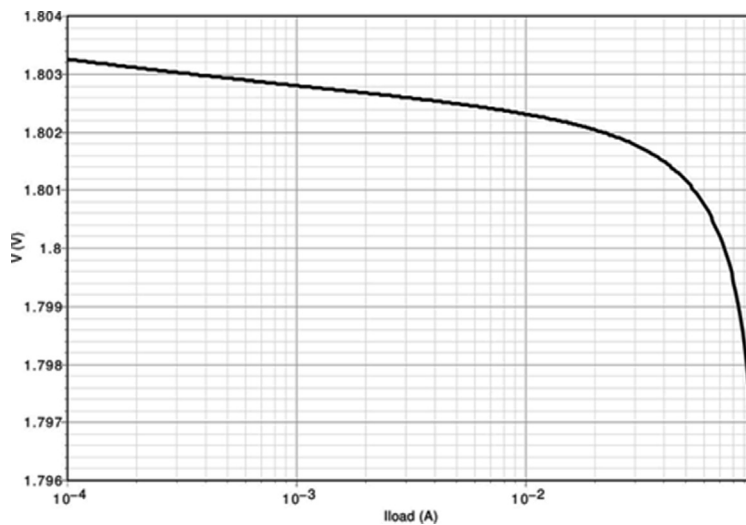

Figure 7. *Load regulation.*

Table 1. *Comparison of different regulators.*

Specifications	(Ming et al., 2012)	(Lovaraju et al., 2013)	(Koay, Chong, And, & Chan, 2013)	This work
[V]	2.5-4	1.4-1.8	1.2	2-3.5
Dropout Voltage [V]	150	200	200	200
[µA]	7	40	13.2	2.3
[mA]	100	100	50	100
[pF]	0-100	100	10-100000	0-100
Settling Time [ns]	150	240	925	300
Line Regulation [mV/V]	1	-	217	5
Load Regulation [mV/mA]	0.08	-	217	0.06
PSR [dB]@10KHz	-	51	-	52
FOM [ps](Ming et al., 2012)	10	96	244	6.9

use of dynamic circuits, as the dynamic biasing proposed, static current consumption is widely decreased improving the figure of merit (FOM) of the circuit.

5. Conclusions

A low-dropout voltage regulator having a low area and power consumption, and a fast transient response is presented. The circuit uses dynamic and adaptive bias for low power operation allowing the power transistor operates in triode region reducing the area. Dynamic bias produces a current increment only during transient operation while adaptive bias increases polarization during and after transient operation for high load current. In both cases, the bias of error amplifier is higher during transient operation allowing high slew-rate. Simulation results using 180 nm standard CMOS technology shows that regulated output can recover within 300 ns for both load and line transient response with a quiescent current of 2.3 µA. Finally, the stability of the regulator is ensured within a range of load capacitance from 0 to 100 pF avoiding the use of external capacitors.

6. Aknowledgement

7. References

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