Ingeniería y Competitividad
Vol 27 (3) 2025 doi: 10.25100/iyc.v27i3.15084

Vol 27 (3)

ISSN
0123-3033
e- 2027-8284

Original Article

Simulation-based comparison of ADRC, PI, and PID controllers on a SEPIC converter: performance and complexity

Comparación basada en simulación de controladores ADRC, PI y PID en un convertidor SEPIC: rendimiento y complejidad

Oscar H. Sierra-Herrera[1] Luis D Patarroyo-Gutiérrez[1] Mario E. González-Niño[2]

[1] Escuela de ingeniería electrónica, Universidad Pedagógica y Tecnológica de Colombia, Tunja, Colombia
[2] Escuela de ingeniería electromecánica, Universidad Pedagógica y Tecnológica de Colombia, Duitama, Colombia.

Abstract

Introduction: SEPIC converters are widely used in power electronics due to their ability to either step up or step down voltage levels. However, their nonlinear behavior and the presence of a right-half-plane zero make it difficult to design fast and stable controllers. This study analyzes the performance of three control strategies applied to a SEPIC converter: Active Disturbance Rejection Control (ADRC), Proportional–Integral (PI), and Proportional–Integral–Derivative (PID).
Objectives: to compare the reference tracking capability, disturbance rejection, and implementation complexity of ADRC, PI, and PID controllers applied to a SEPIC DC-DC converter.
Materials and Methods: simulations were conducted in MATLAB/Simulink by introducing perturbations in both the power source and the output voltage. The performance indices IAE, ITAE, ISE, and ITSE were computed to quantify accuracy, speed, and robustness. The influence of ADRC tuning parameters, such as observer bandwidth and tracking differentiator speed, was also analyzed.
Results: the ADRC controller exhibited the fastest response and best disturbance rejection, although it showed inherent oscillations and higher design complexity. The PI controller achieved a good balance between simplicity and performance, while the PID controller displayed the slowest response but smoother behavior under disturbances.
Conclusions: ADRC is suitable for applications requiring fast and robust control performance. However, PI and PID controllers remain valid alternatives when simplicity or smoother control signals are prioritized.

Keywords: SEPIC converter; ADRC; PI; PID; Disturbance rejection; Non-minimum phase systems; Voltage control; Power system control; Simulation

Resumen

Introducción: los convertidores SEPIC son ampliamente empleados en electrónica de potencia por su capacidad de elevar o reducir voltajes. Sin embargo, su naturaleza no lineal y la presencia de un cero en el semiplano derecho dificultan el diseño de controladores rápidos y estables. Esta investigación analiza el desempeño de tres estrategias de control aplicadas a un convertidor SEPIC: Active Disturbance Rejection Control (ADRC), Proporcional–Integral (PI) y Proporcional–Integral–Derivativo (PID).
Objetivos: comparar el seguimiento de referencia, el rechazo de perturbaciones y la complejidad de implementación de los controladores ADRC, PI y PID en un convertidor SEPIC de corriente continua.
Materiales y métodos: se realizaron simulaciones en MATLAB/Simulink introduciendo perturbaciones en la fuente y en el voltaje de salida. Los índices IAE, ITAE, ISE e ITSE se emplearon para cuantificar precisión, rapidez y robustez. También se analizó el efecto de los parámetros de sintonización del ADRC, como el ancho de banda del observador y la velocidad del diferenciador de seguimiento.
Resultados: el ADRC presentó la respuesta más rápida y mejor rechazo de perturbaciones, aunque con oscilaciones inherentes y mayor complejidad de diseño. El PI logró un equilibrio entre simplicidad y desempeño, mientras que el PID tuvo la respuesta más lenta pero más suave ante perturbaciones.
Conclusiones: el ADRC es adecuado para aplicaciones que exigen control rápido y robusto. No obstante, el PI y el PID siguen siendo alternativas válidas cuando se prioriza la simplicidad o la suavidad en la señal de control.

Palabras clave: Convertidor SEPIC; ADRC; PI; PID; Rechazo de perturbaciones; Sistemas de fase no mínima; Control de tensión; Control de sistemas de potencia; Simulación

How to cite?

Sierra-Herrera OH, Patarroyo-Gutiérrez LD, González-Niño ME. Simulation-based comparison of ADRC, PI, and PID controllers on a SEPIC converter: performance and complexity. Ingeniería y Competitividad, 2025, 27(3)e-20315084

https://doi.org/10.25100/iyc.v27i3.15084

Received: 04/07/25
Reviewed: 03/09/25
Accepted: 21/10/25
Online: 12/11/25

Correspondence

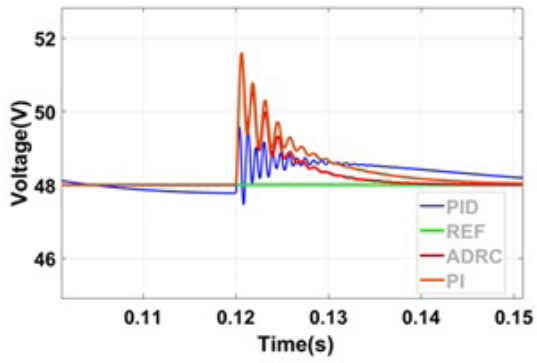
Luis.patarroyo@uptc.edu.co

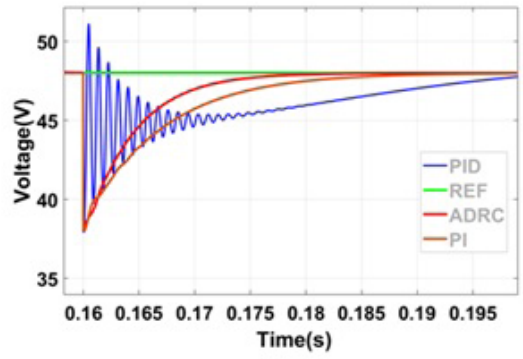
Spanish version

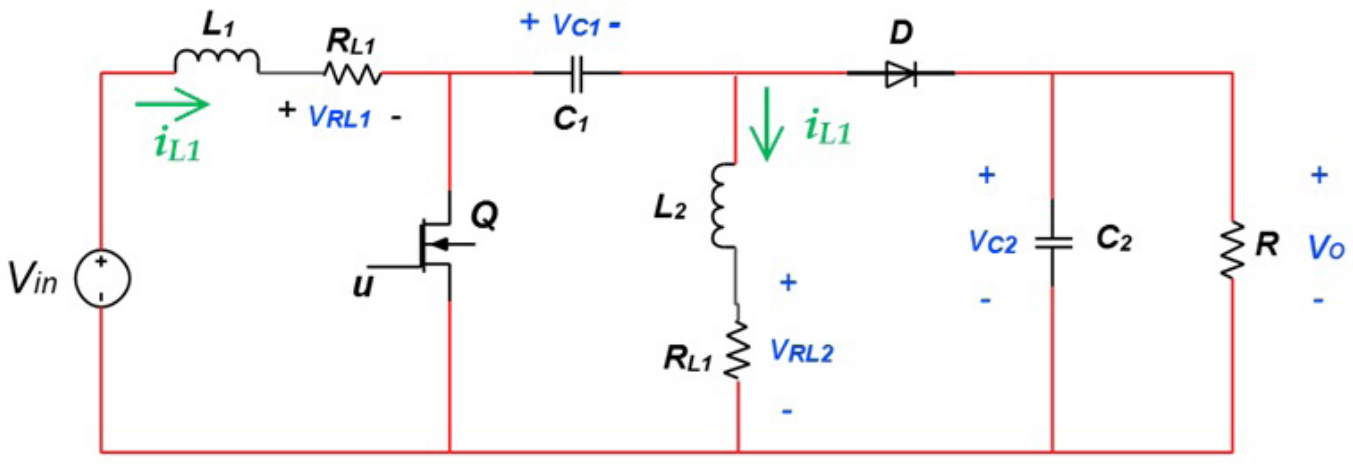
Why was this study conducted?
In recent years, research efforts have increasingly focused on advanced control strategies such as Active Disturbance Rejection Control (ADRC) and on the development of more accurate converter models. This study was conducted to evaluate and compare the performance of ADRC, Proportional–Integral (PI), and Proportional–Integral–Derivative (PID) controllers when applied to a SEPIC DC–DC converter that includes internal resistive losses. The motivation was to determine whether the widely used PID controller remains the most effective and practical solution for DC–DC converters, or if newer strategies such as ADRC can offer superior dynamic performance and disturbance rejection. Because the SEPIC converter exhibits a right-half-plane zero and nonlinear dynamics, it represents a challenging benchmark for control design. The study aimed to provide a fair and quantitative assessment of each controller's performance under identical reference-tracking and disturbance-rejection conditions.

What were the most relevant findings?
ADRC achieved the fastest transient response, the lowest accumulated error, and the best disturbance rejection capability among the evaluated controllers. Quantitatively, ADRC reduced the ITAE by more than 60% compared to PID and by approximately 35% compared to PI, while also achieving a settling time nearly 75% faster than PID. However, ADRC exhibited inherent oscillations in the control signal and required more complex tuning and implementation. The PI controller demonstrated a balanced trade-off between simplicity, robustness, and response speed, making it an attractive option for practical applications. On the other hand, the PID controller provided smoother control actions and reduced overshoot, but its dynamic response was slower. Overall, ADRC outperformed both PI and PID in terms of accuracy and robustness, while PI remained the simplest and most efficient solution for implementations requiring lower computational effort.

What do these findings contribute?
The findings offer deeper insight into the relationship between control performance and design complexity in ADRC, PI, and PID controllers applied to SEPIC converters. By incorporating internal resistive losses into the converter model and evaluating multiple quantitative performance indices (IAE, ITAE, ISE, and ITSE), this work establishes a benchmark for comparing control strategies in power electronic systems. The quantitative results confirm that ADRC can significantly improve transient accuracy, reducing integral error indices by up to 60% but at the cost of higher tuning effort and nonlinear behavior. The outcomes provide valuable guidelines for researchers and engineers seeking to select or design controllers based on the trade-offs between speed, robustness, and implementation simplicity. Ultimately, the study clarifies the practical potential of ADRC as a robust yet complex control alternative and confirms that PI controllers remain a reliable and efficient solution when simplicity and stability are prioritized.







doi: 10.25100/iyc.v27i3.15084

Introduction

DC-DC converters play a key role in modern power electronics due to their use in microgrids, electric vehicles, drones, internet of things (IoT) devices, and portable energy systems (1–3). Among these converters, the Single-Ended Primary Inductor Converter (SEPIC) stands out for its versatility: it can provide output voltages that are higher, lower, or equal to the input, while maintaining non-inverted polarity. This makes it attractive for applications that require flexible voltage regulation. The SEPIC converter also presents advantages such as low output voltage ripple and continuous input current. However, it suffers from limited efficiency, higher component count, and a more complex control structure compared to other topologies such as the buck–boost converter. In addition, its small-signal model exhibits a right-half-plane (RHP) zero, which complicates control design and restricts achievable bandwidth, making the converter a challenging nonlinear system to regulate (4,5).

Traditional Proportional–Integral (PI) and Proportional–Integral–Derivative (PID) controllers are widely used in SEPIC converters due to their simple structure and well-known tuning procedures. For instance, (6) presents a PID controller optimized using a Bat algorithm, achieving a stable output under load and input variations. Nevertheless, classical controllers usually show slow response or limited robustness when dealing with the RHP zero and nonlinear dynamics. These limitations motivate the study of more advanced strategies such as Active Disturbance Rejection Control (ADRC).

ADRC is a control strategy capable of estimating and compensating for both internal and external disturbances without requiring an exact system model. It combines three main elements: the Tracking Differentiator (TD), the Extended State Observer (ESO), and the Nonlinear State Error Feedback (NLSEF) (7–9). The main advantage of ADRC is its robustness against parameter variations and model uncertainties; however, it is characterized by nonlinear behavior, a lack of universal tuning methods, and relatively high implementation complexity. The SEPIC converter, with its non-minimum phase characteristic, provides an excellent benchmark to evaluate the potential of ADRC compared to classical PI and PID controllers. It is hypothesized that ADRC yields a lower ITAE index under input disturbances, resulting in improved transient stability and efficiency for SEPIC-based energy systems. The ITAE (Integral of Time-weighted Absolute Error) criterion was selected as a key performance indicator because it penalizes errors that persist over time, providing a more accurate representation of transient response and control effectiveness compared to traditional indices such as IAE or ISE.

Previous works have explored ADRC in DC-DC converters with promising results. In (10), MATLAB®/ Simulink™ provides a built-in ADRC block for SEPIC converters, achieving good performance but with limited transparency, since parameters cannot be accessed for implementation in digital hardware such as FPGAs. In (11), modifications to the tracking differentiator improved the controller response, although oscillations remained in the control signal. In (12), a simplified SEPIC model was used to implement an ADRC controller, but no comparison was made with conventional controllers. Finally, (13) presented a robust ADRC design based on a fourth-order model, but the work did not report specific tuning parameters or implementation details. These limitations indicate that there

doi: 10.25100/iyc.v27i3.15084

are still no clear guidelines for selecting ADRC, PI, or PID controllers for SEPIC converter control, particularly when considering model accuracy, performance, and implementation complexity.

This work presents a comparative analysis of ADRC, PI, and PID controllers applied to a SEPIC converter modeled with internal resistive losses in the inductors. The study evaluates the reference tracking and disturbance rejection capabilities of each control strategy under identical simulation conditions. Performance is quantified through standardized indices IAE, ITAE, ISE, and ITSE to provide a fair and objective comparison.

Recent studies have addressed similar topics from different perspectives. In (12), Kumar and Ajmeri implemented an ADRC-based control for a SEPIC converter, achieving improved transient response but without analyzing the trade-off between control performance and design complexity. In (14), Patarroyo-Gutiérrez et al. modeled the SEPIC converter considering internal energy losses, providing an accurate physical representation but without applying advanced control strategies such as ADRC. Liu et al. (15) presented an overview of ADRC applications in electromechanical servo drives, emphasizing robustness and implementation challenges, which are also relevant for DC-DC converter control. Unlike these works, this paper integrates both aspects: a SEPIC model that includes internal resistive losses and a quantitative comparison of ADRC, PI, and PID controllers using standardized performance indices (IAE, ITAE, ISE, ITSE), explicitly analyzing the trade-off between control complexity and performance. The analysis also examines whether ADRC represents a practical solution for SEPIC converters considering its higher design and implementation complexity.

This paper is organized as follows:

Section 2 presents the theoretical background of the SEPIC converter and ADRC control. Section 3 describes the design methodology and simulation setup. Section 4 discusses the obtained results, and Section 5 outlines the main conclusions and future research directions.

System Analysis: SEPIC converter and ADRC controller

SEPIC converter

The SEPIC converter is built through the interconnection of energy storage elements, a switch, a diode, a load, and a DC voltage source. Figure 1 shows the converter, including the internal resistance of the inductors.

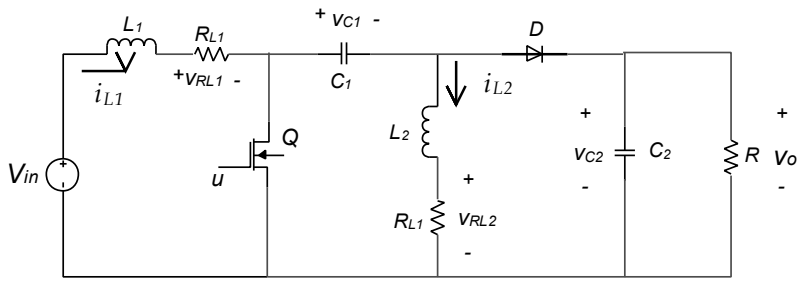


Figure 1. SEPIC Converter

doi: 10.25100/iyc.v27i3.15084

To design the controllers a mathematical model of the converter is needed, in (14), a space state model for the SEPIC converter is presented.

The SEPIC converter model is presented in Equation (1).

$$\begin{aligned} L_1 \cdot \frac{di_{L_1}}{dt} &= V_{in} - R_{L1} \cdot i_{L_1} - (v_{C1} + v_{C2}) \cdot (1-u) \\ C_1 \cdot \frac{dv_{C_1}}{dt} &= i_{L_2} \cdot \alpha + i_{L_1} \cdot (1-u) \\ L_2 \cdot \frac{di_{L_2}}{dt} &= -R_{L2} \cdot i_{L_2} - v_{C1} \cdot \alpha + v_{C2} \cdot (1-u) \\ C_2 \cdot \frac{dv_{C_2}}{dt} &= \left(i_{L_1} - i_{L_2}\right) \cdot (1-u) - \frac{1}{R} \cdot v_{C2} \end{aligned} \quad (1)$$

ADRC Controller

The ADRC controller is presented as a robust control strategy that does not rely on an exact system model. To perform the control actions, ADRC relies on three main components: the Tracking Differentiator (TD), the Extended State Observer (ESO), and the Nonlinear State Error Feedback (NLSEF). Internally, ADRC uses the nonlinear fhan and fal functions. Equations (2) through (8) describe the fhan function (7,15). Here, b_0 represents the plant input gain, r_0 the observer bandwidth, and h_0 the tracking differentiator coefficient.

$$d = h_0 {r_0}^2, a_0 = h_0 v_2;\ y_0 = v_1 + a_0 \quad (2)$$

$$a_1 = \sqrt{d(d + 8|y|)} \quad (3)$$

$$a_2 = a_0 + sign(y)(a_1 - d)/2 \quad (4)$$

$$s_y = (sign(y + d) - sign(y - d))/2 \quad (5)$$

$$a = (a_0 + y - a_2)s_y + a_2 \quad (6)$$

$$s_a = (sign(a + d) - sign(a - d))/2 \quad (7)$$

$$fhan(v2, v2, r_0, h_0) = -r_0 \left(\frac{a}{d} - sign(a)\right) s_a - r_0 sign(a) \quad (8)$$

The fal function is presented at Equation (9).

$$fal(e, \alpha, \partial) = \begin{cases} \frac{e}{\partial^{1-\alpha}}, & |x| \le \partial \\ |e|^{\alpha} sign(e), & |x| \ge \partial \end{cases} \quad (9)$$

doi: 10.25100/iyc.v27i3.15084

Sections 2.2.1 and 2.2.2 provide a brief introduction to the Tracking Differentiator and the Extended State Observer, respectively, and present their mathematical representations.

Tracking differentiator (TD)

It is responsible for generating a smooth reference trajectory and for computing its derivative, allowing the controller to produce gradual transitions and avoid abrupt changes. This helps prevent the amplification of noise measurements, which is a common issue in PID controllers. Various methods exist to generate reference trajectories; in Equation (10), the traditional form presented in (7) is used.

$$\dot{x_1} = x2$$
$$\dot{x}_2 = -r * sign(x_1 - v(t) + \frac{x_2|x_2|}{2r})$$

Extended State Observer (ESO)

The Extended State Observer (ESO) compensates for and estimates disturbances almost in real time. It estimates both the internal states of the system and the unmodeled disturbances. The ESO used is presented in Equation (11); it is the same structure proposed in (7).

$$e = z_1 - y$$
$$fe = fal(e, 0.5, \partial), \quad fe_1 = fal(e, 0.25, \partial)$$
$$\dot{z}_1 = z_2 - B_{01}e$$
$$\dot{z}_2 = z_3 + bu - B_{02}e$$
$$\dot{z}_3 = -B_{03}fe_1$$

The next section describes the methodology used to design the controllers that regulate the output voltage of the converter.

Metodology

The SEPIC converter is implemented in MATLAB code and then called in Simulink as a MATLAB function block. This block can receive and deliver four multiplexed signals, one for each state variable.

Table 1 displays the parameters of the converter used in this work, which operates at a nominal power of 2 kW.

doi: 10.25100/iyc.v27i3.15084

Table 1. Converter parameters.

Parameter	Symbol	Value
Load power	P	2 kW
DC input voltage	V_{in}	90 V
Commutation frequency	f_s	50 kHz
DC output voltage	v_{c2}	48 V
L_1 and L_2 inductors	L_1, L_2	80 µH
Internal L_1 and L_2 inductor resistance	R_{L1}, R_{L2}	50 mΩ
C_1 capacitor	C_1	330 µF
C_2 capacitor	C_2	680 µF
Load (Resistor)	R	1.15 Ω

The implementation of the ADRC controller is carried out in MATLAB®/Simulink™. Figure 2 shows the implemented system. Since the system to be controlled is of type zero, it is necessary to add an integral action to the ADRC.

The converter uses two inputs: the first is a PWM signal that controls the switching of the MOSFET, and the second is the input voltage from the power supply.

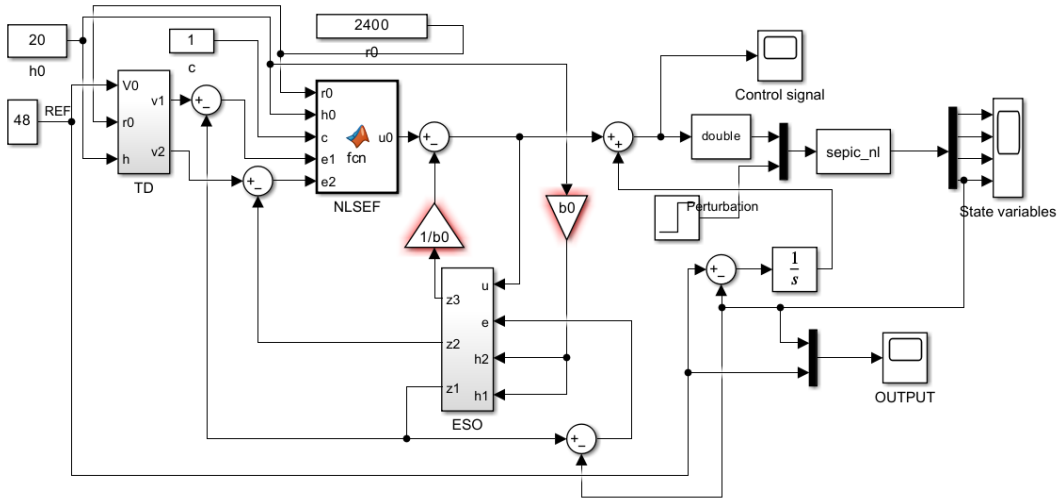


Figure 2. SEPIC converter with ADRC

Figure 3 presents the block diagram of the ESO implementation. The estimator includes the gains b0, Bt01, Bt02, Bt03.

doi: 10.25100/iyc.v27i3.15084

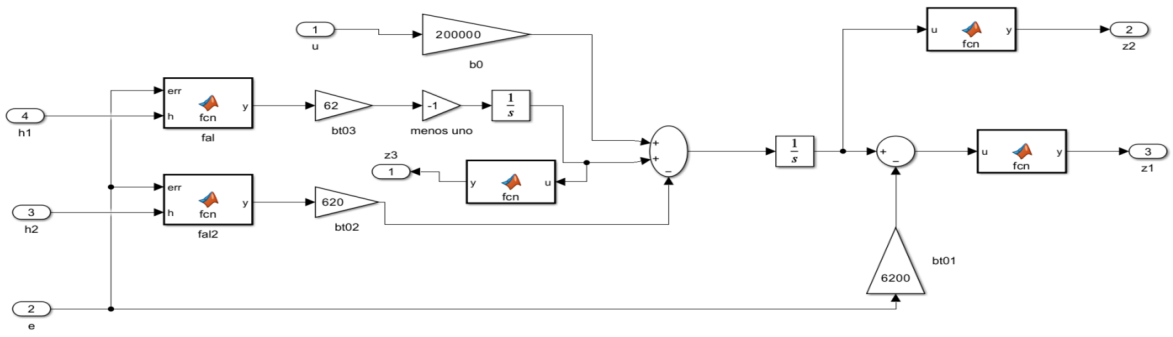


Figure 3. Implemented ESO

The implementation of the Tracking Differentiator shown in Figure 4. This block is responsible for generating a smooth reference trajectory for the NLSEF.

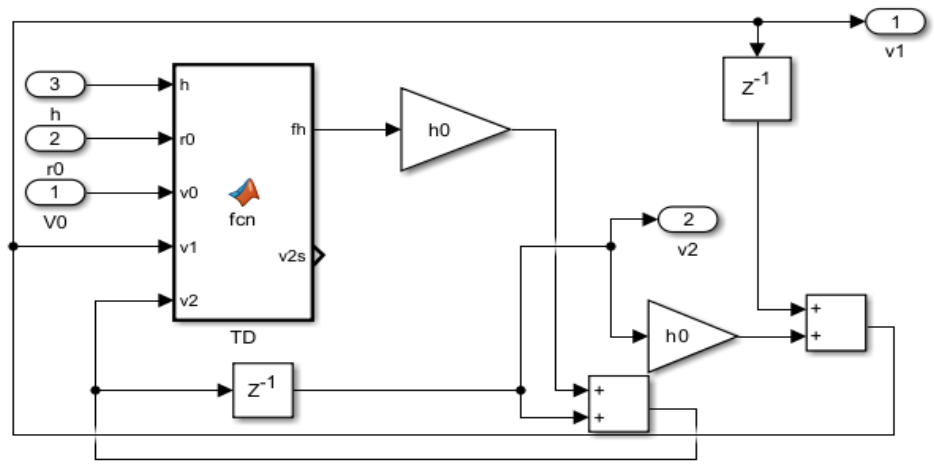


Figure 4. Implemented Tracking Differentiator

PID and PI implementation

Figure 5 shows the closed-loop SEPIC converter with a PI controller, PID has the same implementation.

doi: 10.25100/iyc.v27i3.15084

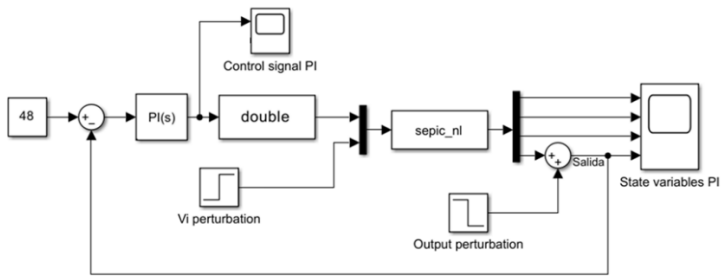


Figure 5. SEPIC converter and PI

The tuning of PI and PID controllers follows the same dynamic model of the SEPIC converter presented in (14), ensuring parameter compatibility with this work's converter configuration. The PI controller parameters are shown in Equations (12) and (13) and the parameters used for the PID controller can be seen in Equations (14), (15) and (16).

$$K_{p1} = 0.00035 \tag{12}$$

$$K_{i1} = 0.686 \tag{13}$$

$$K_{p2} = 0.00035 \tag{14}$$

$$K_{i2} = 0.686 \tag{15}$$

$$K_d = 0.0001 \tag{16}$$

ADRC design

The design of the ADRC begins by calculating the natural frequency of the converter from its model, which in this case is 6200 rad/s. Since the converter has a non-minimum phase zero, it is highly sensitive to noise. In this context, it is known that Bt01 improves the accuracy of the output estimation, Bt02 enhances the dynamic response, and Bt03 increases the speed of disturbance detection, although it also makes the system more sensitive to noise and modeling errors. A fine-tuning process was performed iteratively by adjusting each parameter until a satisfactory transient response was observed, according to ITAE minimization and overshoot reduction criteria. Although empirical, this approach ensured improved dynamic behavior under perturbations, the proposed optimal parameters for the SEPIC converter (Bt01, Bt02, and Bt03) are presented in Equations (17), (18), and (19).

$$Bt01 = w0 = 6200 \tag{17}$$

$$Bt02 = w0/10 = 620 \tag{18}$$

doi: 10.25100/iyc.v27i3.15084

$$Bt03 = w0/100 = 62 \quad (19)$$

Regarding b_0, the literature suggests that it should be the same of slightly greater than the system gain (16). The open-loop gain of this SEPIC converter in the operation point, of the parameters in table 1, is 61000; therefore, b_0 is defined as shown in equation (20):

$$b_0 = g = 61000 \quad (20)$$

The parameter r0 determines the maximum rate of change of the reference signal. In this case, the required rate is 48 V every 20 ms. The value of r0 is shown in Equation (21).

$$r0 = \frac{48}{20mS} = 2400 \quad (21)$$

The parameter C contributes to the stability of the ADRC and improves the system's ability to reject disturbances estimated by the ESO, as it effectively rescales the control input (17). A larger value of C results in a faster system response, while a smaller value leads to slower dynamics. However, if C is too large, it may amplify the noise measurement and lead to undesirable control effort. Therefore, C is typically tuned based on the desired time constant of the closed-loop system. In this case, a target control time of approximately 20 ms is selected, as shown in Equation (22).

$$C = \frac{1}{3 * T} = \frac{1}{3 * 20mS} = 16.67 \quad (22)$$

In this case, with a value of C=16.67, the system reaches the reference; however, the control signal exhibits excessive oscillations in both frequency and magnitude. Therefore, the parameter C was finely tuned. The final value used in this work is presented in Equation (23). With this value, the system reaches the reference in the same amount of time as with C=120, but with a significantly smoother control signal.

$$C = 1 \quad (23)$$

The parameter h0 controls the bandwidth of the tracking differentiator (TD). A larger value increases the responsiveness of the TD, which is necessary in fast systems to avoid phase lag and to ensure accurate derivative estimation (18),(7). MathWorks documentation (19) focuses on tuning the bandwidth of the Extended State Observer (ESO), similar principles apply to the TD. Specifically, it is recommended that the inner components of ADRC (such as the TD and ESO) operate significantly faster than the system dynamics, typically by a factor of 5 to 10. Based on this, the parameter h0 is tuned to a value of 20, as shown in Equation (24).

doi: 10.25100/iyc.v27i3.15084

$$h_0 = 20 \tag{24}$$

Table 2 summarizes the ADRC parameters obtained. Simulations were conducted in MATLAB/ Simulink with a fixed-step solver using the Runge–Kutta method (ode45), integration step of 1e-6 s, and total simulation time of 0.2 s. No anti-windup strategy was implemented for PI/PID controllers.

Table 2. ADRC parameters

Parameter	Value
$Bt01$	6200
$Bt02$	620
$Bt03$	62
b_0	61000
$r0$	2400
C	1
h_0	20

The performance of each controller was evaluated using the time-domain indices IAE, ITAE, ISE, and ITSE, computed from the tracking error $e(t) = v_{ref}(t) - v_{out}(t)$. As shown in Figure 6., the error was integrated over the simulation period T, and in ITAE and ITSE it was multiplied by time t to penalize persistent deviations. This Simulink implementation ensures consistent numerical results and enables a fair comparison among the ADRC, PI, and PID controllers.

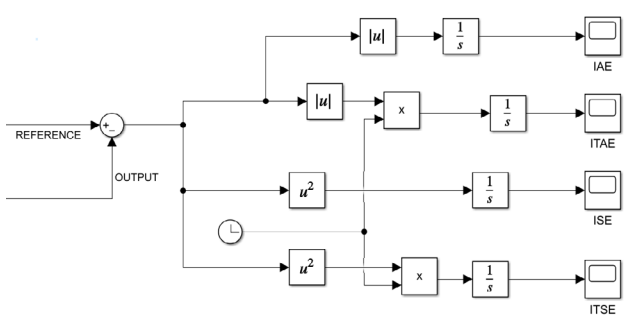


Figure 6. Block diagram used to calculate performance indices (IAE, ITAE, ISE, and ITSE).

Results and discussion

Figure 7 shows the output voltage of a SEPIC converter controlled by ADRC, PI, and PID controllers, reference is at 48 V. At 0.12 seconds, a disturbance is applied to the input power source, causing a sudden change from 90 V to 95 V. Then, at 0.16 seconds, a disturbance of –10 V is applied directly to the system output.

doi: 10.25100/iyc.v27i3.15084

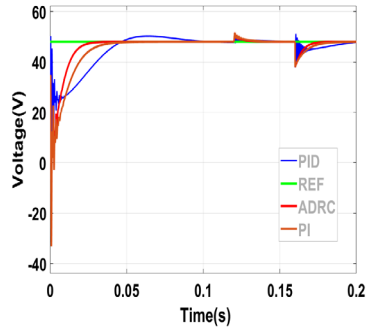


Figure 7. SEPIC Converter Output Voltage with PI, PID, and ADRC Controllers (Time Range: 0–200 ms)

Figure 8 shows the same output as Figure 6, but with a modified time axis ranging from 0 to 0.11 seconds, just before disturbances occur. This zoom-in allows for a detailed analysis of the controllers' reference tracking performance. Parameters such as settling time, overshoot, and steady-state noise can be evaluated. Both the ADRC and PI controllers initially produce negative output voltages due to the non-minimum phase zero characteristic of the SEPIC converter. The PID mitigates the undershoot caused by the non-minimum phase zero, reducing its effect on transient response. However, by control theory, a right-half-plane zero cannot be cancelled by a causal controller. However, it exhibits the slowest response, with a settling time of approximately 100 ms. The ADRC controller settles much faster, around 25 ms, followed by the PI controller, which settles in about 40 ms.

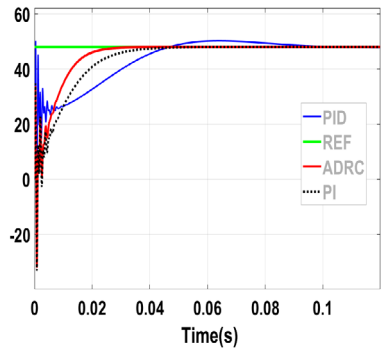


Figure 8. Output Voltage of the SEPIC Converter with PI, PID, and ADRC Controllers (0-120 ms)

Figure 9 shows the response of the controllers to the first disturbance, which is a sudden change in the converter's input voltage from 90 V to 95 V. The ADRC rejects the disturbance in approximately 20 ms, the PI in 25 ms, and the PID in 40 ms. The PID controller exhibits the smallest overshoot, while the PI and ADRC controllers show similar overshoot levels.

doi: 10.25100/iyc.v27i3.15084

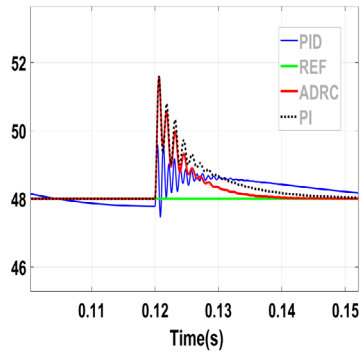


Figure 9. SEPIC Converter Output Voltage with PI, PID, and ADRC Controllers (Time Range: 100-150 ms)

Figure 10 shows the response of the controllers to an output voltage disturbance, consisting of a 10 V dropout. In this case, the ADRC reacts in approximately 15 ms with no overshoot, the PI controller responds in 20 ms, also without overshoot, and the PID controller takes around 40 ms, exhibiting a considerable overshoot.

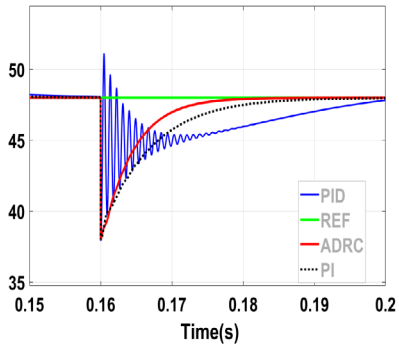


Figure 10. SEPIC Converter Output Voltage with PI, PID, and ADRC Controllers (Time Range: 150-200 ms)

Figure 11 presents the control signals for each of the controllers (in this case, the PWM duty cycle). These signals correspond to the same time window shown in Figure 6, including the initial response, as well as the first and second disturbances. It can be observed that the PID control signal exhibits peaks reaching 0.5 (50% duty cycle), particularly during the disturbances, showing behavior consistent with its overshoot in the output voltage. In contrast, the PI and ADRC controllers produce control signals without overshoot, which is especially evident during the perturbations. Although it may not be clearly visible, the ADRC control signal presents persistent oscillation, this oscillation in ADRC control signal could affect implementation in embedded systems with limited resolution or actuator bandwidth. This behavior, while typical of ADRC, could be mitigated by reducing the TD bandwidth (h_0) or adjusting the ESO gains.

doi: 10.25100/iyc.v27i3.15084

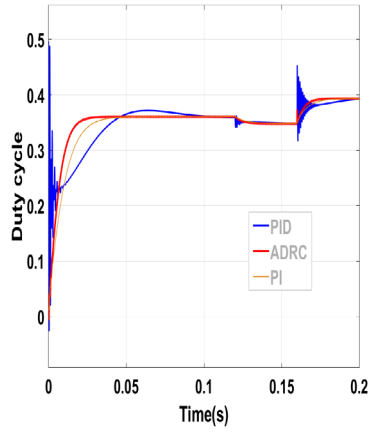


Figure 11. Control signals of PI, PID and ADRC controllers

Additional tests were conducted with different input voltages (50 V, 60 V, 70 V, and 85 V). Since the system exhibited similar behavior in all cases, the corresponding results are not included for the sake of brevity.

Figure 12 presents the IAE index for the ADRC, PI, and PID controllers. It can be observed that the ADRC controller exhibits the lowest accumulated error, followed by the PI controller, while the PID controller performs the worst overall.

In terms of disturbance response, the ADRC and PI controllers behave similarly. The PID controller performs better during the input voltage perturbation; however, during the second disturbance, it accumulates error more slowly but ultimately exceeds the error levels of both ADRC and PI.

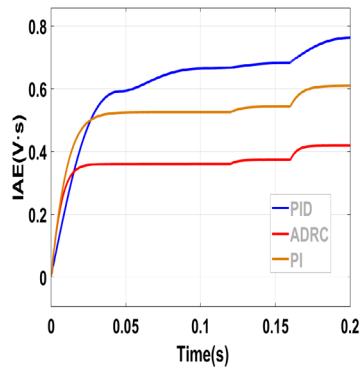


Figure 12. IAE of PID, ADRC, and PI controllers

Figure 13 shows that the ADRC controller accumulates the lowest ITAE error, followed by the PI controller. The PID controller, in contrast, accumulates more than three times the error of the ADRC. During the disturbance events, ADRC demonstrates the best performance, followed by PI, with PID performing the worst.

doi: 10.25100/iyc.v27i3.15084

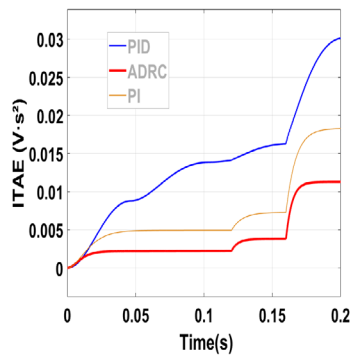


Figure 13. ITAE of PID, ADRC, and PI controllers

Figure 14 shows that the ADRC controller achieves the lowest ISE, followed closely by the PID controller, with the PI controller exhibiting the highest value. During the disturbance events, the PID controller accumulates the least error, followed by ADRC, while PI remains the least effective in this metric.

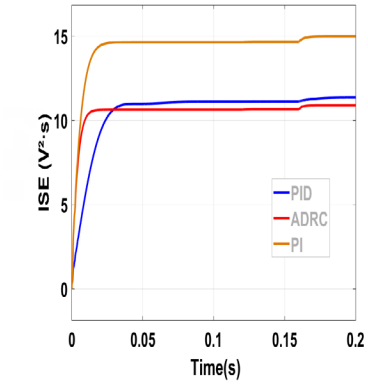


Figure 14. ISE of PID, ADRC, and PI controllers

Figure 15 shows that the ADRC controller accumulates the lowest ITSE, followed by the PI controller, which exhibits nearly twice the error, and finally the PID controller, with more than three times the error.

Regarding the response to disturbances, the PID controller accumulates the least error, followed by ADRC and finally PI shows similar behavior to ADRC but with slightly higher values.

doi: 10.25100/iyc.v27i3.15084

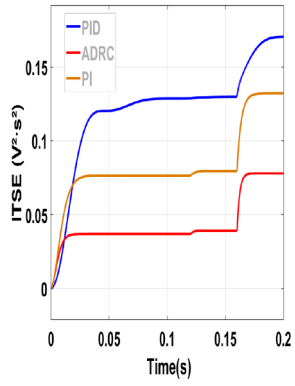


Figure 15. ITSE of PID, ADRC, and PI controllers

From Figures 12 to 15, it can be concluded that the ADRC controller is the most effective in both reference tracking and disturbance rejection, followed closely by the PI controller, which exhibits comparable performance in several metrics. The PID controller performs the worst overall, showing slower reference tracking and higher accumulated error. However, it exhibits a smoother response to perturbations, which may be advantageous in systems with sensitive or limited-actuation hardware.

Conclusions

In this work, an Active Disturbance Rejection Controller (ADRC) was designed and simulated for a SEPIC converter, and its performance was compared against PI and PID controllers. The results show that ADRC provides the fastest reference tracking, the lowest accumulated error, and the best disturbance rejection capability. However, due to the right-half-plane zero inherent to the SEPIC converter, ADRC cannot eliminate the initial undershoot completely. The PID controller mitigates this effect through its derivative action, but with a slower transient response. The PI controller, in turn, offers an intermediate performance with good compromise between speed, simplicity, and stability.

From the analysis, it can be concluded that if fast tracking and strong disturbance rejection are required, ADRC represents the most effective alternative. Nevertheless, its nonlinear structure and tuning complexity make implementation more demanding compared to classical controllers. When design simplicity and reduced computational cost are priorities, the PI controller remains a practical and efficient choice. The PID controller, although slower, provides smoother actuation, which may be advantageous in converters with limited switching bandwidth or sensitive actuators.

The main contribution of this work lies in the inclusion of internal resistive losses in the SEPIC model and in the standardized quantitative comparison of ADRC, PI, and PID controllers through IAE, ITAE, ISE, and ITSE indices. The obtained results serve as a benchmark for controller selection in SEPIC-based power conversion systems and highlight the trade-off between performance and implementation complexity.

doi: 10.25100/iyc.v27i3.15084

Future work will focus on validating these results in a real-time or hardware-in-the-loop (HIL) environment and analyzing the impact of measurement noise and digital implementation constraints on the ADRC structure. In addition, further research could explore adaptive tuning or simplified observer structures to reduce the oscillatory behavior observed in ADRC and improve its applicability to embedded systems.

CrediT authorship contribution statement

Conceptualization - Ideas: Oscar Humberto Sierra Herrera, Luis David Patarroyo Gutiérrez, Mario Eduardo González Niño. Data curation: Oscar Humberto Sierra Herrera Mario Eduardo González Niño. Investigation: Oscar Humberto Sierra Herrera, Luis David Patarroyo Gutiérrez, Mario Eduardo González Niño. Methodology: Oscar Humberto Sierra Herrera, Luis David Patarroyo Gutiérrez, Mario Eduardo González Niño. Project Management: Oscar Humberto Sierra Herrera, Mario Eduardo González Niño. Resources: Oscar Humberto Sierra Herrera, Luis David Patarroyo Gutiérrez, Mario Eduardo González Niño Supervision: Oscar Humberto Sierra Herrera, Luis David Patarroyo Gutiérrez, Mario Eduardo González Niño. Validation: Oscar Humberto Sierra Herrera, Luis David Patarroyo Gutiérrez. Writing - original draft - Preparation: Oscar Humberto Sierra Herrera, Luis David Patarroyo Gutiérrez, Mario Eduardo González Niño. Writing - revision and editing -Preparation: Oscar Humberto Sierra Herrera, Luis David Patarroyo Gutiérrez, Mario Eduardo González Niño.

Financing: does not declare. Conflict of interest: does not declare. Ethical aspect: does not declare.

References

1. Abolghasemi M, Soltani I, Shivaie M, Vahedi H. Recent advances of step-up multi-stage DC-DC converters: A review on classifications, structures and grid applications. Energy Reports. 2025;13:3050–81. doi:https://doi.org/10.1016/j.egyr.2025.02.025

2. Wang R, Feng W, Nordman B, Gerber D, Li Y, Kang J, et al. Technology standards for direct current microgrids in buildings: A review. Renew Sustain Energy Rev. 2025;211:115278. doi:https://doi.org/10.1016/j.rser.2024.115278

3. Venkatesan M, R N, Kacor P, Vrzala M. Bidirectional wireless power transfer: Bridging electric vehicles and the grid through converter analysis, coil topologies, and communication protocol review. Results Eng. 2025;25:103803. doi:https://doi.org/10.1016/j.rineng.2024.103803

4. Yadav A, Verma A. Sepic DC–DC Converter: Review of Different Voltage Boosting Techniques and Applications. 2020;733–9. doi:10.1109/ICIMIA48430.2020.9074897

5. Nazlıgül H, Mert ME, Edis C, Demir BN, Gurdal Y, Elattar KM, et al. Experimental and computational study of a solar-powered electrolysis system with a SEPIC converter for green hydrogen production. Sol Energy. 2025;298:113664. doi:https://doi.org/10.1016/j.solener.2025.113664

doi: 10.25100/iyc.v27i3.15084

6. Khather S, A. Ibrahim M. Modeling and simulation of SEPIC controlled converter using PID controller. Int J Power Electron Drive Syst. 2020;11:833–43. doi:10.11591/ijpeds.v11.i2.pp833-843

7. Han J. From PID to active disturbance rejection control. IEEE Trans Ind Electron. 2009;56(3):900–6. doi:10.1109/TIE.2008.2011621

8. Tu YH, Wang RF, Su WH. Active Disturbance Rejection Control—New Trends in Agricultural Cybernetics in the Future: A Comprehensive Review. Machines. 2025;13(2). doi:10.3390/machines13020111

9. Fareh R, Khadraoui S, Abdallah MY, Baziyad M, Bettayeb M. Active disturbance rejection control for robotic systems: A review. Mechatronics. 2021;80:102671. doi:https://doi.org/10.1016/j.mechatronics.2021.102671

10. The MathWorks Inc. 2024. 2024 [cited 2025 Jun 15]. Design Active Disturbance Rejection Control for SEPIC Converter. Available from: https://la.mathworks.com/help/slcontrol/ug/design-adrc-for-sepic-converter.html

11. Awad N, Humaidi A, Al-Araji A. Modified Tracking Differentiator for Enhancing the Performance of Exoskeleton Knee System Based on Active Disturbance Rejection Control. Univ Baghdad Eng J. 2023;23:69–83. doi:10.33103/uot.ijccce.23.1.6

12. Kumar P, Ajmeri M. Active Disturbance Rejection Control of a SEPIC Converter. Shaw RN, Siano P, Makhilef S, Ghosh A, Shimi SL, editors. Innov Electr Electron Eng. 2024;367–80. doi:https://doi.org/10.1007/978-981-99-8289-9_28

13. Kumar P, Ajmeri M. Robust control of a single-ended primary inductor converter using adrc technique. Eng Res Express. 2023 Dec;6(1):15010. doi:10.1088/2631-8695/ad153e

14. Patarroyo-Gutierrez LD, Gonzalez-Niño ME, Plazas JA. SEPIC Converter: Modeling and Control Considering Internal Energy Losses. Ing y Compet. 2024;26. doi:https://doi.org/10.25100/iyc.v26i1.13016

15. LIU C, LUO G, CHEN Z, DING X. Overview on active disturbance rejection control for electro-mechanical actuation servo drive. Chinese J Aeronaut. 2025;38(7):103292. doi:https://doi.org/10.1016/j.cja.2024.11.002

16. Herbst G, Madonski R. Active Disturbance Rejection Control: From Principles to Practice. 2025. doi:10.1007/978-3-031-72687-3

17. Tian G, Gao Z. Frequency Response Analysis of Active Disturbance Rejection Based Control System. 2007 IEEE Int Conf Control Appl. 2007 Oct;1595–9. doi:10.1109/CCA.2007.4389465

doi: 10.25100/iyc.v27i3.15084

18. Herbst G. Transfer function analysis and implementation of active disturbance rejection control. Control Theory Technol. 2021 Feb;19(1):19–34. doi:10.1007/s11768-021-00031-5

19. The MathWorks Inc. Design Active Disturbance Rejection Control for Boost Converter [Internet]. 2025 [cited 2025 Feb 23]. Available from: www.mathworks.com/help/slcontrol/ug/design-adrc-for-boost-converter.html

doi: 10.25100/iyc.v27i3.15084